Lithographic Manufacturing Techniques for Wafer Scale Integration

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Abstract

Wafer Scale Integration (WSI) lithography is the technique used to fabricate Very Large Scale Integration (VLSI) integrated circuits significantly greater in size than current products. Applications for WSI lithography include large solid state detector arrays, large area liquid crystal displays, high speed mainframe supercomputers, and large semiconductor memories. The lithography technology necessary to manufacture WSI designs is particularly challenging, requiring stringent control of both submicron critical dimensions and accurate alignment of level to level device patterns over large chip areas. The optical step and repeat systems widely used in the semiconductor industry require the stitching of multiple lithography fields to pattern WSI circuits. An analysis of these techniques based on process manufacturability, lithography equipment capability, and tooling costs will be presented in detail.

Field stitching techniques, design considerations, and macrocell grouping techniques which enhance field stitching capability and impact design rules will be described for a mix and match e-beam and 1x optical stepper lithography process. Finally, the proposed lithography process will be experimentally verified using test chip field stitching structures.

1: Introduction

Wafer Scale Integration (WSI) lithography is the technique used to fabricate Very Large Scale Integration (VLSI) integrated circuits significantly greater in size than current products. Applications for WSI lithography include integrated circuits for large solid state detector arrays, large area liquid crystal displays [1,2], high speed mainframe supercomputers [3,4] and large semiconductor memories [5]. Most recently, successful efforts with the VHSIC (Very High Speed Integrated Circuit) program at TRW and Motorola have demonstrated the functionality of the CPUAX (Central Processing Unit-Arithmetic Extended) [2], the world's first monolithic superchip based on WSI technology. In contrast to current generation VLSI circuits which are as large as 300 mils per side, the CPUAX design is 1500 mils per side and incorporates over 4 million active devices. The CPUAX is an advanced central signal processing system with potential applications in medical diagnosis, plant process control and complex imaging [6].

The lithography technology necessary to manufacture WSI designs is particularly challenging. Successful WSI lithography demands stringent control of both submicron critical dimensions and accurate alignment of level to level device patterns over chip areas many times larger than existing commercial monolithic integrated circuits (IC). Because of the large WSI

4

chip dimensions, the lithography equipment field size is an additional important requirement. The lens field size limitation for step and repeat systems can necessitate field stitching multiple optical exposure images [7]. Figure 1 illustrates this common dilemma associated with field constraints for a WSI circuit. For the case of a 2000 by 2000 mil circuit, a total of sixteen separate stepper fields are required to be stitched together. This occurs because optical stepper fields dimensions are typically on the order of 350 to 450 mils per side. While this field size is adequate for VLSI applications, it is clearly deficient for WSI designs. Since a WSI circuit must then be composed of separate optical fields, the precise relative positioning of each field, or alignment error, is critical. If not properly controlled, alignment errors can severely limit both design flexibility and process yields on such WSI circuits.

Although implementation of optical field stitching techniques poses a formidable challenge in manufacturing environments, it appears necessary in future Dynamic Random Access Memory (DRAM) technologies. Based on the existing evolutionary pace of stepper lens field sizes and resolution [8], as well as the historical trends in DRAM integration [9], it appears that future advanced optical lithography will require field stitching below 0.3 micron linewidths with chip sizes greater than 25 mm per side for the production of a 64 megabit DRAM [10]. Researchers at Fujitsu recently illustrated field stitching, also denoted as blocking, of 8 optical fields together as a viable approach for fabricating a 64 megabit DRAM, and compared this approach to the use optical-phase shifting [11] to increase device packing density [12]. Hence, utilization of field stitching techniques offers the potential of extending the usefulness of optical steppers.

A methodology utilizing a mix-and-match approach of optical 1x lithography and e-beam lithography currently used at TRW for WSI technologies will be discussed. The inherent field stitching techniques, and design considerations which enhance the achievable field stitching capability will also be described. A comparative cost analysis of WSI tooling costs, WSI wafer throughput, and WSI tooling requirements will be presented to illustrate the tradeoffs among the various lithography systems. Finally, the representative results of the proposed lithography process will be presented using test chip field stitching structures.

2: Alignment of Field Stitching

A number of different lithography tools could be considered for WSI lithography. These include e-beam direct write on wafer, optical step and repeat reduction printing, optical step and repeat 1x printing and scanning optical 1x. The technical equipment performance that plays an essential role in WSI technology are resolution, image field size and level to level alignment capabilities. A previous evaluation of these tools has shown that optical step and repeat printing offers advantages over other systems in terms of cost versus performance [12]. An additional consideration is that optical step and repeat systems are the industry standard for semiconductor fabrication.

All step and repeat optical systems require field stitching techniques to achieve WSI lithography. This implies that the alignment error is critical in comparison of systems for WSI applications. The common major error components can be expressed as the interfield error (σ_{IEF}), which denotes field stitching alignment error for typical WSI circuit applications [13]. For WSI lithography it is also necessary to consider a maximum interfield stitching error (MISE), which is expressed in equation (1). The total alignment error for a given field is approximated as 3 times σ_{IEF}. This implies that twice this value is required to account for relative errors of two fields that are in opposite directions:

$$MISE = 6 \, \sigma_{IEF} \tag{1}$$

Figure 2a shows the worst case alignment of vertical lines of nominal width (L) crossing a field boundary where the top field is misaligned to the left by $3\sigma_{IEF}$ and the bottom field is

misaligned to the right by the same distance. When using positive tone photoresists [14] for optical pattern transfer , this causes a reduction in linewidth in the area of the horizontal overlap of each field (2O). As a result, the interfield minimum line (L) must be greater than the intrafield minimum line (L_m) by the MISE:

$$L = L_m + MISE \qquad (2)$$

Similarly, the space (S) between the lines appears to be larger in the area of field overlap by the MISE. However, if the overlap (O) is substantially diminished as shown in figure 2b, a reduced space (S_m) can occur between the lines at the overlap edge points. The minimum overlap required to prevent (S_m) from being less than (S) can be determined using Pythagorean's theorem with the second order terms disgarded:

$$O = 3\sigma_{IEF} + (S*3\sigma_{IEF})^{0.5} \qquad (3)$$

Equations (2) and (3) show clearly that the overall RMS alignment capability directly impacts the minimum pitch (line plus space) and the field overlap required for interfield connections for WSI circuits.

3:WSI Architecture

WSI design methodology has been widely discussed in the literature [5]. However, the choice of lithography systems can also impact the design process. A conservative approach to WSI methodology is to construct the WSI circuit using a discrete number of circuit building blocks [15], or macrocells, as shown in the top diagram on figure 3. Each macrocell is a self contained VLSI circuit that can be individually fabricated and functionally verified to reduce testing complexity for the final WSI chip. In addition, WSI chip defect density can be overcome using redundant macrocells for high single chip yield [15]. In the top diagram, the individual macrocell is placed in a single stepper field and can therefore be designed to take advantage of maximum lithography capabilities without consideration for field stitching rules. The larger the field of the lithography tool, the more macrocells can be placed and routed without stitching. Using this approach, only interconnect layout rules between the macrocells crossing field boundaries is impacted by field stitching. These rules can be expressed in terms of the pitch of the interconnect. It was shown in equations (2) and (3) that only linewidth is adversely affected during field stitching if sufficient field overlap is maintained. Therefore, the effective circuit packing density across field boundaries is inversely proportional to the square of the line and space. The density can be expressed in terms of a normalized packing density (Dn), normalized minimum pitch (Pn) and normalized interfield error (σn) as:

$$D_n = 1/(P_n + 6\sigma_n)^2 \qquad (4)$$

It is apparent that normalized density (D_n) is maximized when operating at the minimum pitch with the minimum interfield alignment error. Both the pitch and the alignment error are determined by the choice of lithography tools. This emphasizes the point that the lithography tool with highest resolution and minimum alignment error should be considered first for WSI applications, to maximize design rule flexibility and reduce the resulting WSI circuit size. Figure 3 illustrates the tradeoffs with respect to design rule flexibility and macrocell size for various aggressive design schemes. The middle and bottom diagrams show macrocells being placed across field boundaries. The most flexible approach for layout is to allow all device levels in a macrocell to cross boundaries. However, these levels are then impacted by field stitching design rules. An intermediate approach is to allow only some levels to cross the boundary. This minimizes the impact on macrocell size but maintains flexible macrocell placement.

The macrocell approach also suggests a useful comparative indicator for lithographic pattern density based on a linear pixel count:

$$\text{Linear Pixel Count} = \text{Field Area} / (\text{Resolution} + \text{Alignment Error})^2 \qquad (5)$$

For example, the CPUAX superchip corresponds to a linear pixel count of approximately 1.3 million. The absolute size of the chip in millimeters would be dependent on the lithography tool assuming the circuit design rules are adjusted to take advantage of system resolution and registration accuracy.

4:WSI Manufacturing

Once the design of a WSI circuit is completed, the appropriate tooling for the selected lithography equipment must be obtained. For steppers the tooling consists of patterned chrome on quartz reticles, where each individual reticle contains the pattern device structures for a single device layer. For all reduction step and repeat systems, a single reticle is necessary for each unique optical exposure field. Consequently, the requirement for multiple unique fields for a WSI circuit implies multiple reticles are needed for each device level. This is in stark contrast to conventional requirements for VLSI processing were only one reticle is necessary per device level.

The lithography tooling represent a sizable financial investment and directly impacts the manufacturability of the WSI circuit. A comparison of the reticle set costs for five representative optical steppers is shown in figure 4a. It is apparent that costs can vary dramatically depending on the linear pixel count and the selection of the lithographic equipment. The ASM stepper shows the lowest reticle costs over a large range of linear pixel count. This is primarily due to the superior resolution and registration of this system. The Canon stepper is a close second as a result of its large lens field size.

The increased number of reticles required for the steppers adversely impacts the WSI wafer throughput (figure 4b), which is the typical VLSI or single pass throughput divided by the number of reticles per level. This occurs because every wafer must be processed through the stepper once per reticle on a given process level, and hence multiple times per process level. This severely lowers throughput for large WSI circuits. In addition to the logistical difficulty of multiple wafer passes, there is a significantly larger probability of incurring processing errors resulting in the need for lithography reworks. While the Nikon, Canon and ASM systems all have similar throughput for small linear pixel counts, the ASM leads for large WSI chips. This is again due to the resolution and registration capabilities which reduce the number of reticles required for each process level.

5:Methodologies and Results

TRW's approach to WSI lithography is based on a mix-and-match methodology, using both a Hitachi HL-700 direct write e-beam and an Ultratech Systems 1500 1x optical stepper. As reported in a previous study [13], the 1x optical stepper provides an excellent compromise capability in terms of technical equipment performance, manufacturability, throughput and tooling costs. The e-beam complements the 1x stepper well when used for process levels requiring critical half micron feature control, such as the polysilicon gate level, and also levels requiring accurate alignment control, such as contact and first metal levels. In addition to these levels, the e-beam is used for patterning an accurate predevice registration level. This level provides three important objectives for the TRW WSI process. First, it delineates an accurate registration level to minimize field stitching errors for fields that are subsequently patterned on the 1x stepper. This is essential since the initial pattern placement error accuracy of the e-beam is significantly better than that of the 1x stepper. Secondly, it defines robust alignment targets for both lithography tools that are useable throughout the whole process [16]. Finally, using a

predevice level single alignment scheme minimizes the total RMS (Root Mean Square) alignment budget [16].

An example of metal interfield stitching is shown in Figure 5a by Scanning Electron Micrographs (SEM) of etched metal interconnect. The design rules used for this example are 3.5 micron interfield linewidth (L) and 3.0 spacewidth (S) using a field overlap (2O) of 1.0 microns. This represents minimal stitching error with little visual indication of the stitching boundary. An example of MISE is illustrated in Figure 5b with an error of 0.28 microns. For both these examples a high contrast photoresist process was used, followed by an anisotropic dry etch process with high resist to metal selectivity. It is apparent that the effect of double lithographic exposure in the overlap region causes no observable linewidth variation.

6:Conclusions

The proper selection of a lithography tool is essential for successful WSI technology. Based on design considerations, it is recommended to select a lithography tool with the highest resolution and minimum registration performance.

Design considerations are also implicitly coupled to the choice of lithography tool, and depending on the design rules employed can dramatically affect the resulting WSI circuit size. The conservative approach is based on constructing a WSI circuit using a discrete number of macrocells contained within a stepper field. This approach concurrently maximizes the use of the stepper capabilities and eliminates all field stitching except for the less critical interconnect lines.

Finally, there are major benefits of these WSI lithography techniques and design methodologies. First, utilization of field stitching can effectively extend the usefulness of optical steppers, such as meeting future DRAM requirements. Also, field stitching techniques can enhance circuit design flexibility by eliminating lithography equipment field constraints.

At TRW, a WSI lithography process based on a mix-and-match approach using a 1x optical stepper and a direct write e-beam is currently being used to maximize lithography capability. Utilizing this approach, the world's first monolithic based superchip, the CPUAX, was fabricated.

7:References

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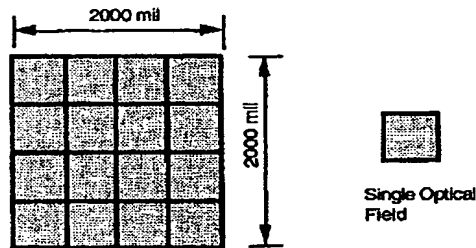
Figure 1: Example of a 2000 by 2000 mil WSI circuit constructed using multiple optical image fields on a step and repeat system. Precise relative placement of adjacent fields , or field stitching, is a critical in the lithography process.
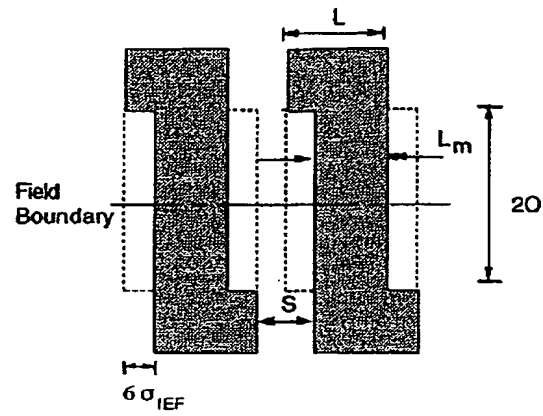
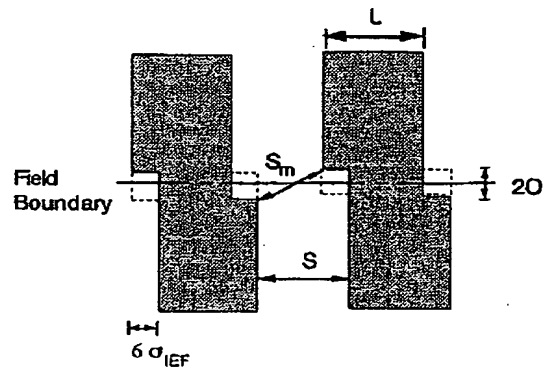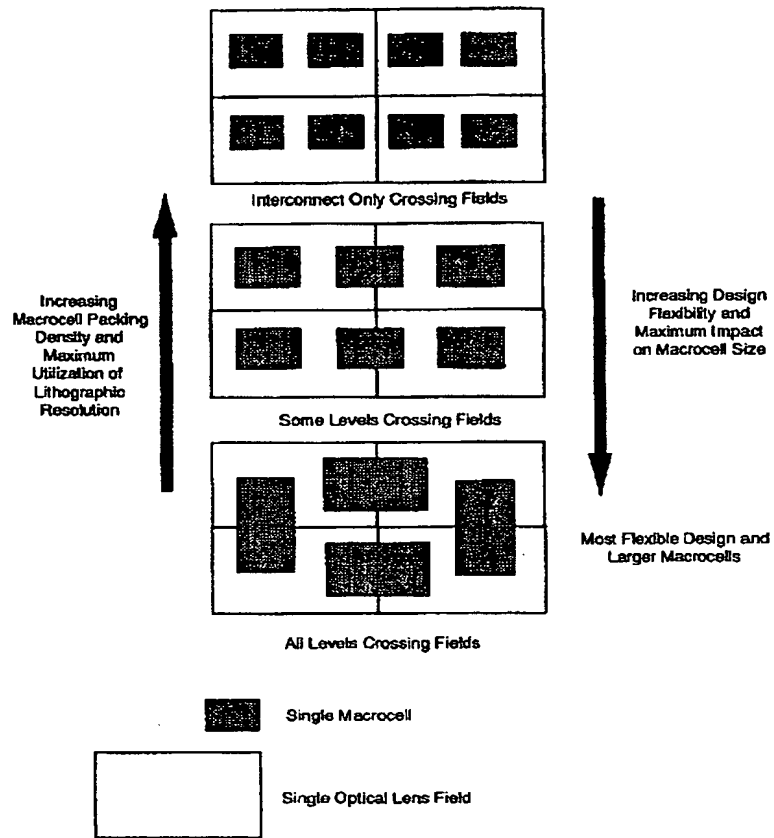**Figure 2a: Example of field stitching interconnect lines with a large overlap.**

Figure 2b: Example of field stitching interconnect lines with a minimum overlap.

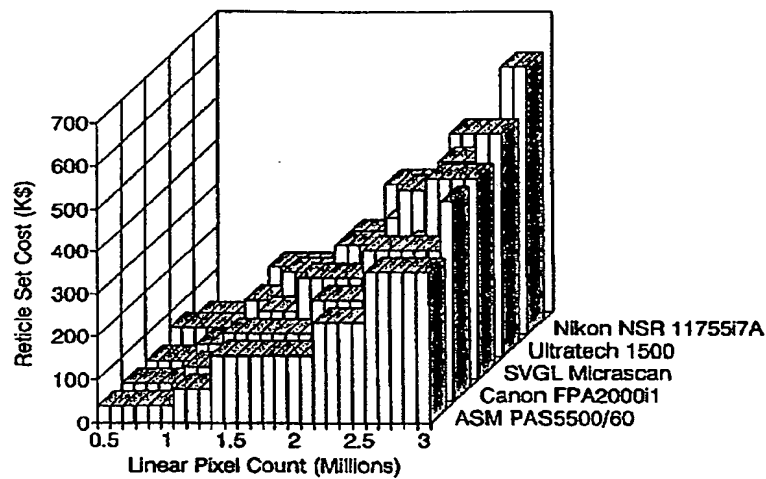## Figure 3: WSI Design Schemes For Optical Lithography

Interconnect Only Crossing Fields

Some Levels Crossing Fields

All Levels Crossing Fields

Increasing
Macrocell Packing
Density and
Maximum
Utilization of
Lithographic
Resolution

Increasing Design
Flexibility and
Maximum Impact
on Macrocell Size

Most Flexible Design and
Larger Macrocells

Single Macrocell

Single Optical Lens Field

Figure 4a: Reticle set cost as a function of linear pixel count for five optical step and repeat systems.
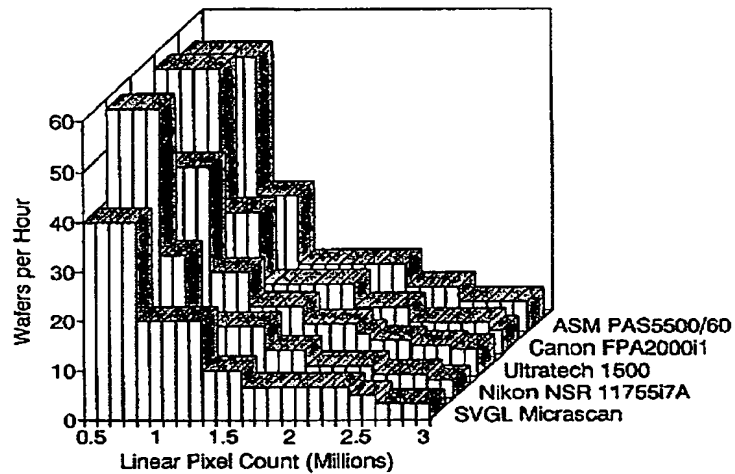
Figure 4b: Wafers per hour as a function of linear pixel count for five optical step and repeat systems.

Optical Field Boundary ⟶
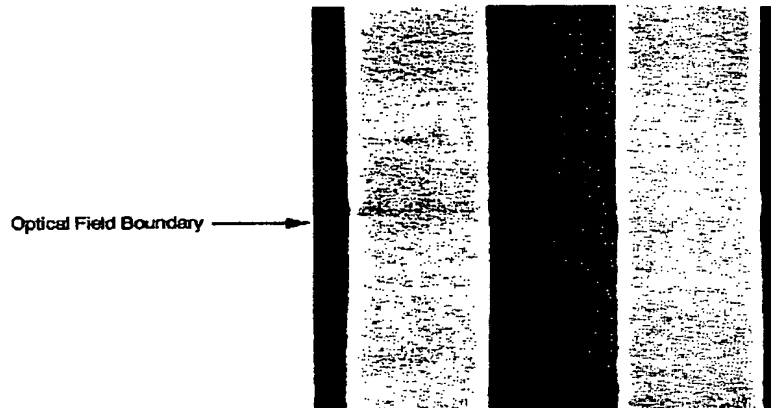
Figure 5a: SEM of metal interconnect using a minimum overlap stitched across a horizontal field boundary which illustrates a minimum interfield error. The design rules are 3.5 micron interfield linewidth, 3.0 micron spacewidth and field overlap of 1.0 microns at a magnification of 7000x.

Optical Field Boundary ⟶
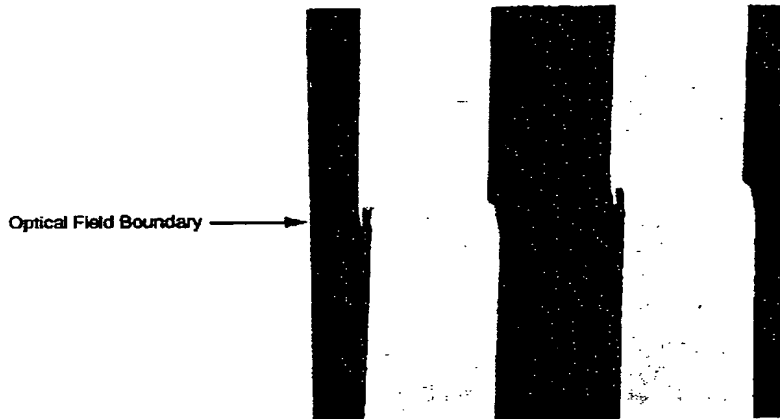
Figure 5B: SEM of metal interconnect using a minimum overlap stitched across a horizontal field boundary which illustrates a maximum interfield error. The design rules are 3.5 micron interfield linewidth, 3.0 micron spacewidth and field overlap of 1.0 microns at a magnification of 7000x.